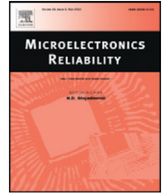
Microelectronics Reliability 55 (2015) 2263–2268

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr



Process optimization of RTA on the characteristics of ITO-coated GaN-based LEDs

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ARTICLE INFO

Article history:
Received 17 April 2015
Received in revised form 15 July 2015
Accepted 22 July 2015
Available online 4 August 2015

Keywords:
Light emitting diodes
Rapid thermal annealing
Gallium nitride
Indium tin oxide

ABSTRACT

We present a detailed study on the optimization of rapid thermal annealing (RTA) on GaN-based light emitting diodes (LEDs). 14 mil × 28 mil GaN-based LED chips are fabricated with indium tin oxide (ITO) layer treated by RTA under various temperatures and times. Through the optical and electrical property analyses of ITO film, it is found that the transmittance and sheet resistance are improved after RTA process due to the better ITO crystallization and bigger grain size, compared with ITO treated by conventional furnace annealing. By employing electroluminescence measurement for the LED chips with RTA treatment, the forward voltage is found to be low as a result of low sheet resistance and contact resistance, and light output power (LOP) is high due to high ITO transmittance and good current density uniformity. Under RTA temperature of 550 °C and time of 3 min, the optimized LOP and forward voltage at 60 mA injection current are 71.2 mW and 2.97 V, respectively. Moreover, the reliability of the chips with RTA is better than those with furnace annealing.

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1. Introduction

With the development of GaN-based light emitting diodes (LEDs), more and more attentions have been focused on their use in backlights for liquid–crystal displays and cell phones, exterior automotive lighting, traffic signals, etc. [1,2]. Due to high acceptor activation energy, the free hole concentration is low in p-GaN, indium tin oxide (ITO) is used as the current spreading layer for its low optical absorption coefficient and high electrical conductivity. However, although significant progress has been made in the growth and processing technology of LEDs, poor Ohmic contact at ITO/p-GaN interface is still a problem. Large contact resistances result in high chip forward voltage, low light extraction efficiency and increase LED junction temperature, which eventually lead to the degradation of GaN-based LEDs [3,4]. In order to obtain optimum performance of conventional GaN-based LED chips, it is important to realize low resistance thermal stability and uniform Ohmic contact between ITO and p-GaN.

In the fabrication process of GaN-based LED chips, after ITO films are deposited on top of p-GaN by evaporation in vacuum circumstance, they are usually treated by furnace annealing to form Ohmic contact [5], during which the heating rate is low and parasitic resistance induced by poor contact at the ITO/p-GaN interface is high. In order to obtain good electrical properties, other annealing methods should be considered to guarantee good contact. In the past few years, rapid thermal annealing (RTA) has gained acceptance as the mainstream thermal process in semiconductor manufacturing industry. During RTA process, the wafer could be heated up and cooled down quickly, thus reducing the solid-state diffusion of dopants introduced in the previous fabrication steps, leading to a low parasitic resistance. Some publications have reported the application of RTA on LEDs [6,7], however the researchers mainly focus on the device performance of LED chip with RTA treatment. The mechanism of optical and electrical property improvement due to RTA still needs to be further studied.

In this paper, we presented a detailed investigation on the RTA process applied in the GaN-based LED chip fabrication, the mechanism of RTA applied on LEDs was analyzed, and various temperatures and annealing times were chosen to optimize RTA condition. In addition, devices with furnace annealing were made for the sake of comparison. After RTA treatment, the electrical and optical properties of ITO films under various RTA conditions were studied.

2. Experimental details

The GaN epilayers used in this study were grown on (0001) sapphire substrates by metalorganic chemical vapor deposition using hydrogen as the carrier gas, and trimethylgallium, trimethylindium, and ammonia were used as Ga, In, and N sources, respectively. Silane and biscyclopentadienyl magnesium were used as n-type and p-type dopants, respectively. The LED epitaxial structure was as follows: GaN buffer layer was deposited on the sapphire at a temperature of 520 °C, followed

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http://dx.doi.org/10.1016/j.microrel.2015.07.043
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by 2.5 μm thick undoped-GaN and 2 μm thick Si-doped n-GaN at 1150 °C; the undoped InGaN/GaN multiquantum well (MQW) active region was grown at 780 °C, and finally, a 150 nm thick Mg-doped p-GaN epilayer was grown at 1050 °C; and the InGaN/GaN MQW active region consisted of 11 pairs of 3 nm thick InGaN well layer and 9 nm thick GaN barrier layer. The as-grown LED wafers were subsequently annealed at 750 °C in N_2 ambient temperature to activate Mg in p-GaN.

To guarantee the performance uniformity, LED wafers from the same epitaxial run were selected to perform the following chip processes, which were implemented by using standard chip processing techniques including photolithography, inductively coupled plasma (ICP) etching, and electron-beam (E-beam) evaporation, etc. After photolithography, these wafers were partly etched by ICP until the n-GaN layer was exposed. Prior to ITO deposition, the samples were dipped into sulfuric acid hydrogen peroxide solution (H_2SO_4:H_2O_2 = 3:1) for 2 min, and rinsed in running deionized water to clean the p-GaN surface. Afterwards, the ITO film with a thickness of 110 nm was deposited on these samples in E-beam evaporation chamber under a vacuum pressure of 3×10^{-6} Torr, with processing temperature of 300 °C and deposition rate of 1 Å/s. Then the wafers with the ITO film were rapidly annealed at various temperatures (400–700 °C) and annealing times (1–10 min) in N_2 atmosphere, while one wafer was subjected to furnace annealing under standard industrial condition (500 °C, 10 min, N_2 atmosphere). Finally, Cr/Au was evaporated to form p-type and n-type electrodes. By utilizing grinding and polishing, these wafers were thinned to 120 μm thickness, then scribed and broken into 14 mil × 28 mil GaN-based LED chips, thus the chip fabrication was finished. Fig. 1 gives the real picture and schematic cross-section view of GaN-based LED chip.

3. Results and discussion

3.1. Characteristic of ITO film

During the deposition of ITO film, the glass substrates were loaded in the E-beam evaporation chamber accompanied with GaN-based LED wafers to monitor the sheet resistance and transmittance of ITO film, which are important electrical and optical parameters to characterize ITO quality. After deposition, we tested the ITO film on glass substrate by using standard four-point probe technique and spectrophotometer. The sheet resistance (average of several measurements at different positions on the sample) and transmittance of ITO film prior to annealing were measured as 9.2 Ω/□ and 91.2% (at 460 nm), respectively. Transmittance was normalized with respect to the glass substrate. Then, the glass substrates with the ITO films and other LED wafers were rapidly thermally annealed at various temperatures and times in N_2 ambient temperature. Temperature ramping speed was 20 °C/s, and N_2 flow rate was 7 L/min. At the same time, in order to compare the effect of furnace annealing to that of RTA, one piece of glass with the ITO film and one LED wafer were annealed in conventional furnace under standard industrial condition instead of RTA.

After annealing process finished, the parameters of ITO films at different annealing conditions were measured again by testing ITO films on glass substrates. Figs. 2 and 3 give the transmittance and sheet resistance of ITO films under different RTA temperatures and annealing times, respectively. It is seen that at a certain annealing time, the transmittance increases slightly in low temperature range, and then decreases after the temperature exceeds 550 °C. While the sheet resistance decreases firstly, and then increases. In comparison, the transmittance and sheet resistance of ITO film after furnace annealing are 98.3% and 12.5 Ω/□, respectively.

The as-deposited ITO films are amorphous, and annealing can arrange atoms to form stable polycrystalline films. With the increase of annealing temperature, the degree of ITO crystallization is enhanced [8]. Moreover, the stress of ITO films formed during deposition process is better released [9]. These lead to high Hall mobility, as well as improved transmittance due to the reduced light absorption. At the same time, the neutral tin atoms diffuse to occupy some host lattice sites. This will increase the cations, and then oxygen vacancies increase. Due to the high Hall mobility and increment of oxygen vacancies after annealing, the conductivity of ITO film improves. When the annealing temperature is over 550 °C, lattice distortion will decrease Hall mobility, which then plays a more important role in the variation of ITO conductivity than the increment of oxygen vacancies, thus the conductivity decreases [10]. Moreover, the lattice distortion reduces the transmittance due to light absorption.

The sheet resistance determines the conductivity of ITO film, especially for the in-plane conductivity, which influences the current uniformity in InGaN/GaN MQW. Sheet resistance is affected significantly by electron mobility. To further understand sheet resistance variations, scanning electron microscope (SEM) measurements are carried out for all of these samples. Fig. 4 presents the SEM micrographs for ITO films with furnace annealing, as well as with RTA under different temperatures at 3 min annealing time. It can be seen that the grain size is smaller for ITO film annealed by furnace than those by RTA. With increasing RTA temperature, ITO grain evolves from small size to big one, then small size again. Since the annealing temperature is from 400 °C to 700 °C (the time is from

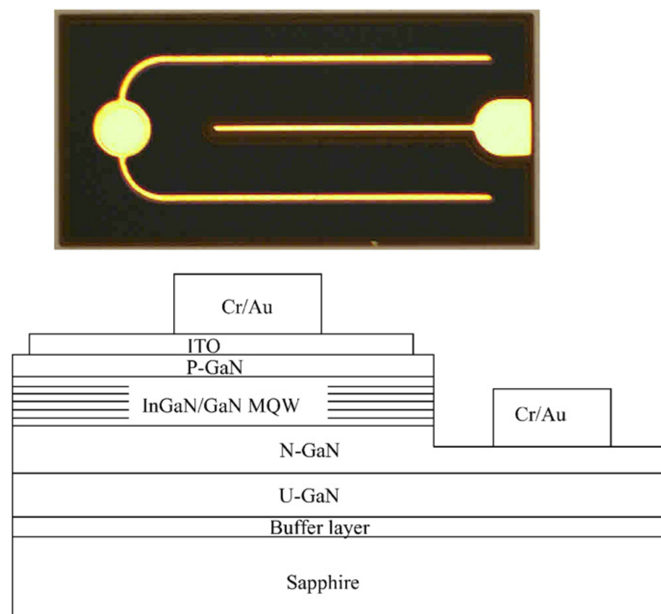

Fig. 1. Optical micrograph (upper) and schematic cross-section view of GaN-based LED chip (bottom).

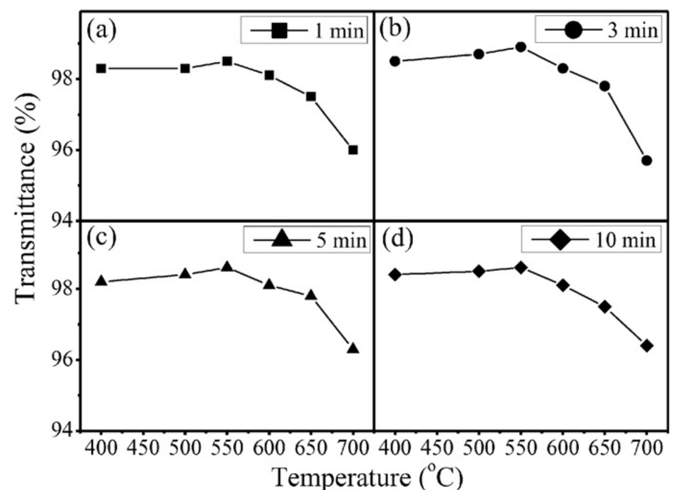

Fig. 2. Transmittance of ITO films under various RTA temperatures at annealing times of (a) 1 min, (b) 3 min, (c) 5 min and (d) 10 min.

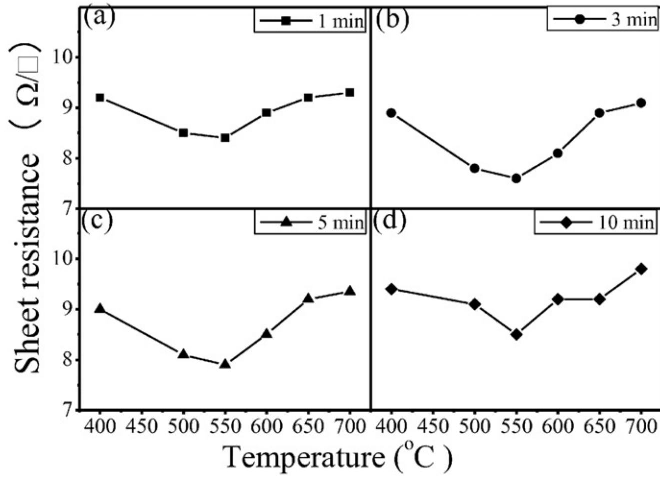

Fig. 3. Sheet resistance of ITO films under various RTA temperatures at annealing times of (a) 1 min, (b) 3 min, (c) 5 min and (d) 10 min.

1 min to 10 min), under which the crystal grain has formed and grain boundaries become apparent. Suppose that grain boundary scattering functions as the main scattering mechanism for ITO films after RTA treatment [11], sheet resistance R_s can be expressed as [12]:

$$R_s = 1/nq\mu_g t \tag{1}$$

where

$$\mu_g = (\delta q)/(2\pi m_n^* KT)^{\frac{1}{2}} \exp\left(-\frac{\phi_b}{KT}\right). \tag{2}$$

Here n is the free electron concentration, q is the electron charge, μ_g is the electron mobility dictated by grain boundary, t is the film thickness, δ is the grain size, m_n^* is the electron effective mass, ϕ_b is the grain boundary potential barrier, K is the Boltzmann constant and T is the absolute temperature. For the small grain size, electrons are frequently scattered by the boundary when passing through ITO film, which results in the low electron mobility. It is evident that the sheet resistance is approximately inversely related to electron mobility, so the conductivity of ITO film is better after RTA treatment than that after furnace annealing. For other annealing times, ITO grain exhibits the same evolution with temperature, and the lowest sheet resistance (7.6 Ω/□) and highest transmittance (98.9%) can be obtained when RTA condition is 550 °C at 3 min.

3.2. Optical and electrical properties of LED chips

In order to investigate the optical and electrical properties of LED chips, room-temperature electroluminescence characteristics were measured by injecting 60 mA DC current into the fabricated LED chips on wafers. Fig. 5(a) and (b) displays the light output power (LOP) and forward voltage (V_F) for LED chips on the wafers under different ITO annealing conditions, respectively. Note that different wafers were subjected to different annealing conditions. There were thousands of LED chips on each wafer, and LOP and voltage values were the average values for the chips on each wafer. From Fig. 5(a), it is found that under fixed annealing time, LOP increases with temperature first, and then decreases in high temperature range. However, LOP exhibits different tendencies with time at different RTA temperatures. In total, LOP varies from 68.8 mW to 71.6 mW (for the chip with ITO furnace annealing, LOP is 69.2 mW), the variation of which is affected by ITO transmittance and sheet resistance. High transmittance means low light loss when the photons generated in InGaN/GaN MQW pass the ITO layer, thus leading to high LOP. However, high sheet resistance indicates bad in-plane conductivity of ITO, resulting in the insufficient current spreading, which intensifies the current crowding [13,14]. As a result, non-uniform current density occurs in InGaN/GaN MQW. The resulting local device heating and low photon generation efficiency of active

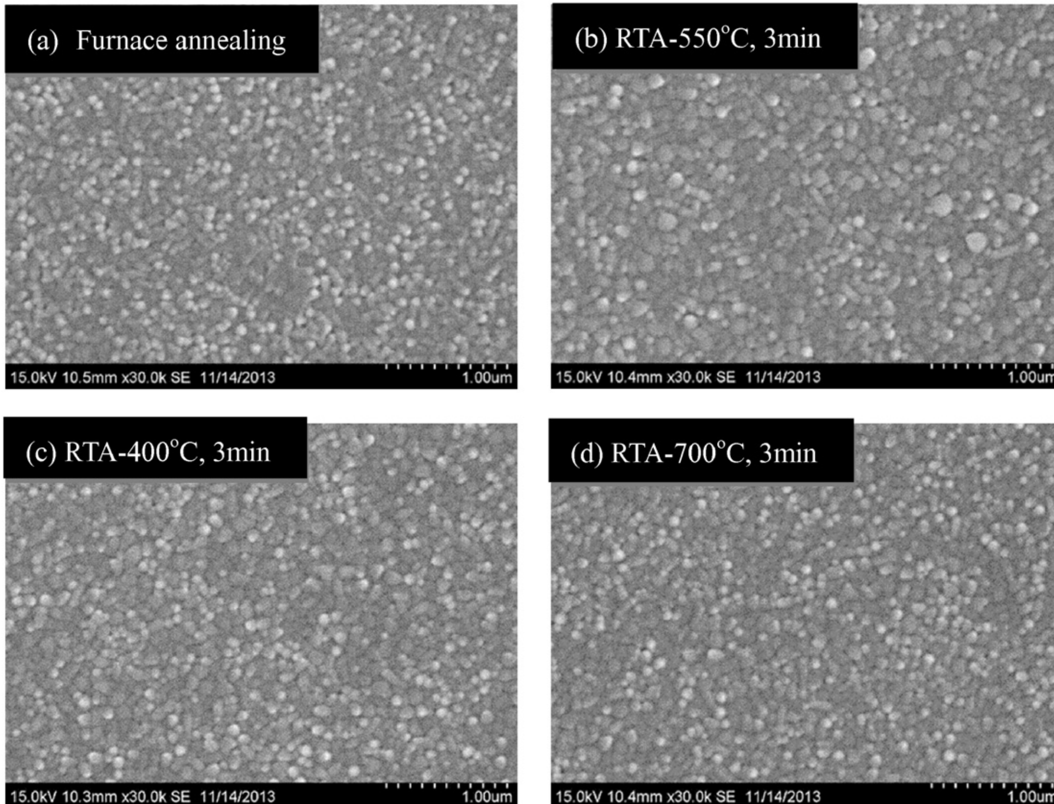

Fig. 4. SEM micrographs for ITO films treated by (a) furnace annealing, (b) RTA-550 °C, 3 min, (c) RTA-400 °C, 3 min, and (d) RTA-700 °C, 3 min.

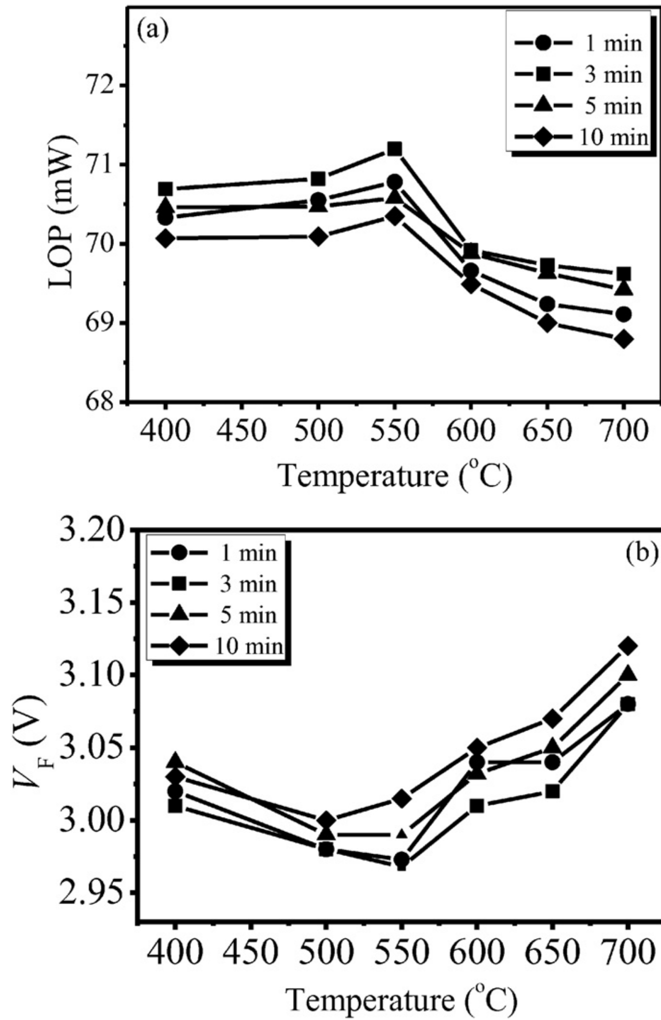

Fig. 5. LOP (a) and V_F (b) of LED chips treated with different RTA conditions.

region induce low LOP. Therefore, we can see that the variation of LOP correlates to that of ITO transmittance and sheet resistance as shown in Figs. 2 and 3.

It is seen from Fig. 5(b) that with increasing RTA temperature, V_F decreases first and then increases. For comparison, the average V_F of LED chips on LED wafer with furnace annealing is 3.06 V. It is known that V_F is impacted by sheet resistance of ITO, as well as the interface status between ITO layer and p-GaN. To further analyze V_F variation under different annealing conditions, we employed the square transmission line model (s-TLM) to study the specific contact resistance at the interface between ITO layer and p-GaN. Fig. 6(a) shows the schematic view of TLM array structure fabricated in LED wafers, the area of each TLM pad is 200 μm (L) × 700 μm (w), the distance between two neighbor TLM pads is marked as d_i (i = 1,2… 5), and the width of the outermost square p-GaN is 720 μm (z). Due to that (z–w) ≪ w, according to s-TLM model [15,16], the total resistance R_i between the contacts is expressed as:

$$R_i = \left(\frac{R_{sh}}{z}\right) \cdot d_i + 2 \cdot R_c, \;\; i = 1, 2\ldots5 \tag{3}$$

$$\rho_c = \frac{R_c^2 \cdot z}{R_{sh}}. \tag{4}$$

Here, R_{sh} is the sheet resistance of p-GaN layer, R_c is the contact resistance, and ρ_c is the specific contact resistance. To get the influence

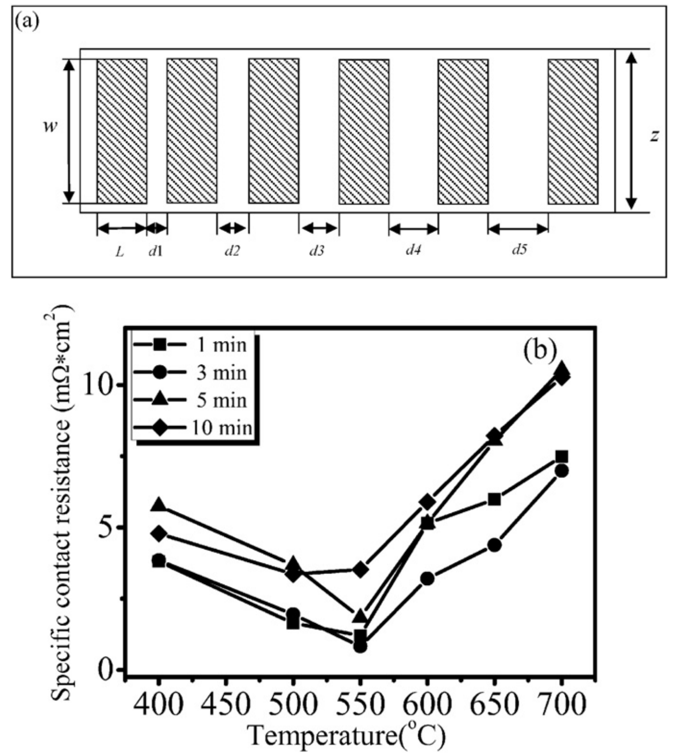

Fig. 6. (a) Schematic view of processed TLM patterns; (b) specific contact resistance of the ITO/p-GaN interface as functions of RTA temperatures and times.

of various RTA conditions on ρ_c, current–voltage measurements were taken on TLM patterns. Through lineally fitting the experimental data, R_{sh} and R_c can be obtained, and then ρ_c can be calculated for the chips under different ITO annealing conditions, as shown in Fig. 6(b).

We find that ρ_c has a similar relationship with RTA conditions as that of V_F, indicating that besides ITO sheet resistance, ρ_c plays an important role in forward voltage change after ITO annealing. During RTA process, gallium atoms diffuse out from p-GaN to the ITO contact and create gallium vacancies, and indium atoms diffuse from the ITO contact to gallium vacancy sites in addition to the diffusion of Sn and O to GaN, therefore forming a mixed interfacial layer at the ITO/p-GaN interface composed of $In_xGa_{1-x}N$, $In_xGa_yO_z$, etc., which could reduce the barrier height and decrease contact resistance [17]. For high annealing temperature and long annealing time, the excessive intermixing of materials at the interface due to excessive annealing will increase the barrier width, resulting in high contact resistivity [18]. It is also seen that under long annealing time, ρ_c is higher at most annealing temperatures than that under short annealing time, indicating that good contact has already been formed for short time annealing, while long annealing duration induces the contact deterioration. In the case of furnace annealing, the interface materials could not be intermixed ideally due to the low temperature ramping rate, thus leads to a high ρ_c (7.5 mΩ cm^{-2}). Through the optical and electrical property investigations of the chips, the highest LOP (71.2 mW) and lowest V_F (2.97 V) can be obtained when ITO is rapidly thermally annealed at 550 °C for 3 min.

To study the optical and electrical performances of LED chip at different driving currents, we tested the LOP–current and V_F–current relationships for the chips with RTA under 550 °C at different annealing times, accompanied with that of furnace annealing, as presented by Fig. 7. In this measurement, unpackaged chips were used and all of these chips were measured on wafers. It demonstrates from Fig. 7(a) that at different currents, LOP for the chips with RTA annealing is higher than that of the chips with furnace annealing, showing better optical characteristic of

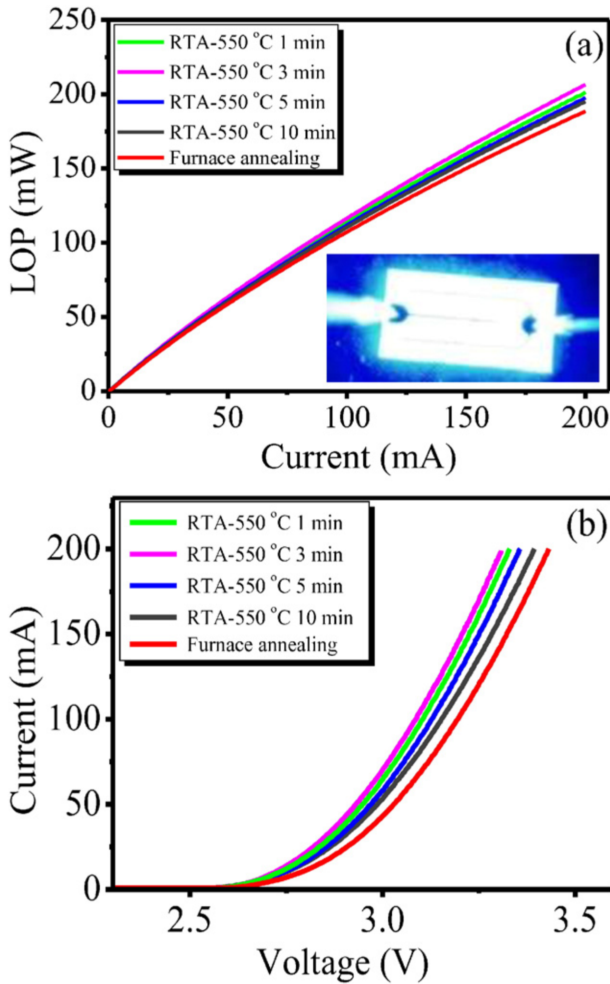

Fig. 7. LOP–current (a) and V_F–current (b) relationships for the chips with RTA under 550 °C at different annealing times. The inset shows the emission image of LED chip with a driving current of 5 mA.

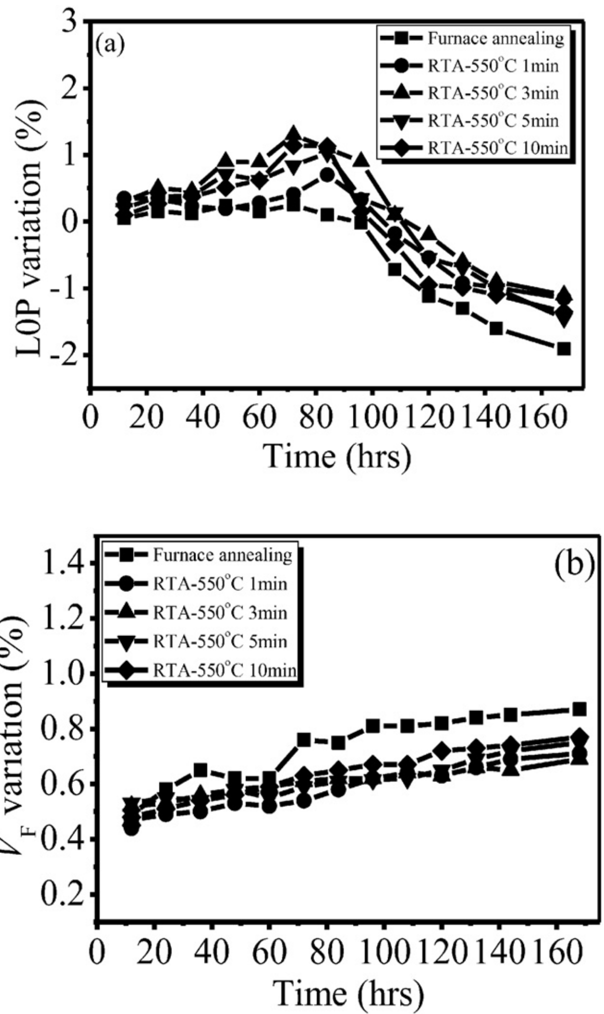

Fig. 8. Normalized LOP (a) and V_F (b) variations of the chips during accelerated aging test under 90 mA driving current at 85 °C of ambient temperature.

LED chip after RTA treatment. The inset shows the electroluminescence emission image of LED chip at an injection current of 5 mA. Fig. 7(b) exhibits that with the increase of injection current, the voltage increases smoothly, furthermore, the turn-on voltage for the chips under RTA treatment is a little lower than that of furnace annealing, due to the lower series resistance resulting from good ITO/p-GaN contact.

3.3. Reliability of LED chips

After these wafers were ground and polished, they were scribed and broken into separate chips. To carry out the accelerated aging test, we package the chips in the transmitter optical can-type to avoid the impact induced by packaging process as much as possible. The performance of light output was measured by calibrating an integrating sphere with a Si photodiode on the package device, which can collect the light emitted in any direction from the LED. Fig. 8 presents the LOP and V_F variations (normalized to the initial values) of the chips during accelerated aging test under 90 mA driving current at 85 °C of ambient temperature. It is found that after 168 h aging, LOP of the chips with furnace annealing decreases by ~2%, larger than the LOP decrement for the chips with RTA. At the same time, for the chips with furnace annealing, V_F increases slightly with aging time due to the series resistance increment induced by degradation process. While for the chips with RTA treatment, electrical worsening is less than that with furnace annealing as a result of better contact property. Both optical decay and electrical worsening measurements imply the thermal stability of ITO film treated by RTA.

4. Conclusions

The mechanism and optimization of RTA process applied on GaN-based LEDs have been studied. Employing the optical and electrical measurements, we found that the transmittance and sheet resistance of ITO films treated by RTA are better than those treated by furnace annealing. The electroluminescence analysis for GaN-based LED chips with RTA demonstrates that under an annealing temperature of 550 °C at 3 min, the optimized light output power and forward voltage for the fabricated 14 mil × 28 mil chips with 60 mA injection current are 71.2 mW and 2.97 V, respectively, due to that the current density is uniform and the specific contact resistances at the interface between ITO layer and p-GaN are low. In addition, the reliability of the chips with RTA is better than those with furnace annealing.

Acknowledgments

This work was supported by National Major Basic Research Project of 2012CB934302, research fund for the doctoral program of Shanghai University of Engineering Science under contract 201308, Shanghai Youth College Teachers Training Program of ZZGJD13023, and Shanghai "YangFan" project (no. 14YF09500).

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